

REMARKS

Reconsideration of this application as amended is respectfully requested.

In the Office Action, claims 1-26 and 34-36 were pending and rejected. In this response, claims 1, 4, 7, 12, 18, 22, and 34 have been amended to particularly point out and distinctly claim, in full, clear, concise, and exact terms, the subject matter which Applicants regard as their invention. No new matter has been added.

Objection to drawings

The claims, as amended, do not require a capacitor connected in parallel to two or more pass gates. Therefore, Applicants submit that no correction of drawing is required and respectfully request the objection be withdrawn.

Rejections under 35 U.S.C. § 112

In the Office Action, claims 1-11 were rejected over 35 U.S.C. § 112. In this response, claims 1 and 7, as amended, requires “two or more pass gates coupled in parallel to each other, wherein a first terminal of each of the two or more pass gates is coupled to the conductor and a second terminal of the each of the two or more pass gates is coupled to the capacitor”. Applicants submit that the claims are supported by the drawings and the specification. Applicants respectfully request withdrawal of the rejection of the claims.

Rejections under 35 U.S.C. § 103

Claims 1, 2, 7-10, 18-21, 34, and 35 were rejected under 35 U.S.C. 103(a) as being unpatentable over Lin, US 6,868,504 (hereinafter “Lin”) in view of Lo et al., US Publication 2003/0102894 (hereinafter “Lo”).

Claim 1, as amended, recites:

1. A programmable delay cell comprising:
a capacitor coupled to a low supply rail;
a conductor coupled to an output of said programmable delay cell; and
**two or more pass gates coupled in parallel to each other, wherein a
first terminal of each of the two or more pass gates is coupled to
the conductor and a second terminal of the each of the two or
more pass gates is coupled to the capacitor.** (Emphasis added)

Applicants submit that Lin and Lo fail to disclose at least “two or more pass gates coupled in parallel to each other, wherein a first terminal of each of the two or more pass gates is coupled to the conductor and a second terminal of the each of the two or more pass gates is coupled to the capacitor” as required in claim 1. Lin discloses a delay line for use in phase locked loop and delay locked loop circuits (Figure 3a). The Office Action admits that Lin fails to disclose two or more pass gates. There is no description or drawing in Lo that shows this limitation as required in claim 1. Therefore, Lin and Lo, even if combined, would still fail to teach all the elements of claim 1. At least for the foregoing reason, Applicants submit that claim 1 is not obvious over Lin and Lo. Applicants respectfully request that the rejection for claim 1 be withdrawn.

Regarding claim 2, the Office Action alleges that Lin discloses “wherein an impedance of each of said pass gates is to be controlled by a respective control signal”. Applicants respectfully disagree. Lin describes that load can be adjusted through operation of switches 47-54 (column 3, line 67 to column 4, line 17). There is no mention of pass gates and control signals. Therefore, Applicants submit that Lin does not disclose the limitation. At least for the foregoing reasons, claim 2, depending from claim 1, is allowable over Lin and Lo. Applicants respectfully request that the rejection for the claim 2 be withdrawn.

Claims 7, 18, and 34, as amended, require “two or more pass gates coupled in parallel to each other, wherein a first terminal of each of the two or more pass gates is coupled to the

conductor and a second terminal of the each of the two or more pass gates is coupled to the capacitor.” Applicants would like to submit that Lin and Lo fail to teach at least this limitation.

At least for the foregoing reason, Applicants believe that claims 7, 18, and 34 are not obvious over Lin and Lo. Claims 8-10, 19-21, and 35, depending from claims 7, 18, and 34, are also allowable for at least the same reason. Applicants respectfully request that the rejections for the claims be withdrawn.

Claim 3 and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin in view of Lo and Sharp, US 4,584,492 (hereinafter “Sharp”). Claim 3 and 36, depending from claims 1 and 34 respectively, are not obvious over Lin and Lo. As set forth above, Lin and Lo do not disclose “two or more pass gates coupled in parallel to each other, wherein a first terminal of each of the two or more pass gates is coupled to the conductor and a second terminal of the each of the two or more pass gates is coupled to the capacitor”. Sharp does not cure the deficiency of Lin and Lo. Moreover, claim 3 requires a variable impedance transistor. Sharp describes a circuit comprising transistors (transistors 14-16, 21-23) including transistor 23 that is driven by a feedback signal (Sharp, Figure 1). All the transistors are n-channel enhancement mode transistors (Sharp, col. 3, line 49-51). Sharp shows a circuit comprising many components to compensate for temperature and power supply changes. All the transistors in Sharp are of specific sizes. For example, transistors 21, 20, and 23 must be identical to transistors 14, 15, and 16 (Sharp, col. 4, line 21-25). Sharp requires all transistors to be preselected and matched so that the compensation circuit is operable. Sharp does not disclose “a variable impedance transistor” as required in claim 3. At least for the foregoing reasons, Applicants believe that claim 3 and 36 are not obvious over Lin, Lo, and Sharp. Applicants respectfully request that the rejections for the claims be withdrawn.

Claims 4-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin in view of Sharp. Claim 4, as amended, recites:

4. A programmable delay cell comprising:
a conductor coupled to an output of said programmable delay cell;
a switch transistor coupled to the conductor; and
a variable impedance transistor coupled to a high supply rail and to a
source terminal of the switch transistor, wherein an impedance of
said variable impedance transistor is to be determined by a control
signal. (Emphasis added)

Applicants would like to submit that, Lin and Sharp fail to disclose at least “a variable impedance transistor coupled to a high supply rail and to a source terminal of the switch transistor, wherein an impedance of said variable impedance transistor is to be determined by a control signal” as required in claim 4. The Office Action admits that Lin does not disclose “a variable impedance transistor”. Sharp fails to cure the deficiency. Detailed remarks with respect to claim 3 are incorporated herein by reference.

Claims 12-16 and 22-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin in view of Sharp. Claim 12 and 22, as amended, requires “a switch transistor coupled to the conductor” and “a variable impedance transistor coupled to a high supply rail and to a source terminal of the switch transistor, wherein an impedance of said variable impedance transistor is to be determined by a control signal”. Applicants would like to submit that both Lin and Sharp fail to disclose at least this limitation. Detailed remarks with respect to claim 4 are incorporated herein by reference.

At least for the foregoing reasons, Applicants believe that claim 4, 12, 22 are not obvious over Lin and Sharp. Claims 5-6, 13-16, and 23-26 depending from claims 4, 12, and 22 are also allowable for at least the same reason. Applicants respectfully request that the rejections for the claims be withdrawn.

Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lin, Lo, Ahmad, Indian Patent No. 633/DEL/2003 (hereinafter “Ahmad”), and Nakahata, U.S. Patent No. 4,528,634 (hereinafter “Nakahata”).

Claim 11, depending from claim 7, is not obvious over Lin and Lo. Ahmad and Nakahata fail to cure the deficiency of Lin and Lo with respect to claim 7. Furthermore, claim 11 requires “one or two registers coupled to said output buffer to store a first value that determines the source driving impedance of said output buffer and to store a second value that determines the sink driving impedance of said output buffer.” The Office Action alleges that Ahmad in view of Nakahata discloses the limitation. Applicants respectfully disagree. Ahmad shows a pull-up predriver, a pull-down predriver, and configuration bits (Ahmad, Figure 2). There is no association between configuration bits and driving impedance values of output pin (DATAOUT) in Ahmad. Therefore, Ahmad does not teach “a first value that determines the source driving impedance” and “a second value that determines the sink driving impedance of said output buffer”. Nakahata also is silent with respect to disclosing “a first value that determines the source driving impedance” and “a second value that determines the sink driving impedance of said output buffer”.

At least for the foregoing reasons, Applicants believe that claim 11 is not obvious over Lin, Lo, Ahmad, and Nakahata. Applicants respectfully request that the rejection for the claim be withdrawn.

Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lin, Sharp, Ahmad, and Nahakata.

Claim 17, depending from claim 12, is allowable over Lin and Sharp. Ahmad and Nakahata fail to cure the deficiency of Lin and Sharp with respect to claim 12. Additionally, claim 17 requires “one or two registers coupled to said output buffer to store a first value that

determines the source driving impedance of said output buffer and to store a second value that determines the sink driving impedance of said output buffer”. As discussed, Ahmad and Nahakata fail to teach the limitation. Detailed remarks with respect to claim 12 are incorporated herein by reference.

At least for the foregoing reasons, Applicants believe that claim 17 is not obvious over Lin, Sharp, Ahmad, and Nakahata. Applicants respectfully request that the rejections for the claim be withdrawn.

CONCLUSION

In view of the foregoing, Applicants respectfully submit the present application is now in condition for allowance. If the Examiner believes a telephone conference would expedite or assist in the allowance of the present application, the Examiner is invited to call the undersigned attorney at (408) 720-8300.

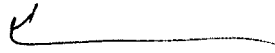
Please charge Deposit Account No. 02-2666 for any shortage of fees in connection with this response.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN

Date: _____

4/8/09



Michael J. Mallie
Attorney for Applicant
Reg. No. 36,591

1279 Oakmead Parkway
Sunnyvale, California 94085-4040
(408) 720-8300